IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Lee**	§	
	§	Group Art Unit: **2189**
Serial No. **10/809,594**	§	
	§	Examiner: **Gu, Shawn X.**
Filed: **March 25, 2004**	§	
	§	
For: **Method to Allow PCI Host Bridge (PHB) to Handle Pre-Fetch Read Transactions on the PCI Bus Which Access System Memory Through Translation Control Entry (TCE) Table**	§	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

35525
PATENT TRADEMARK OFFICE
CUSTOMER NUMBER

APPEAL BRIEF (37 C.F.R. 41.37)

This brief is in furtherance of the Notice of Appeal, filed in this case on January 16, 2007.

A fee of $500.00 is required for filing an Appeal Brief. Please charge this fee to IBM Corporation Deposit Account No. 09-0447. No additional fees are believed to be necessary. If, however, any additional fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447. No extension of time is believed to be necessary. If, however, an extension of time is required, the extension is requested, and I authorize the Commissioner to charge any fees for this extension to IBM Corporation Deposit Account No. 09-0447.

REAL PARTY IN INTEREST

The real party in interest in this appeal is the following party: International Business Machines Corporation of Armonk, New York.

RELATED APPEALS AND INTERFERENCES

With respect to other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no such appeals or interferences.

STATUS OF CLAIMS

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-7, 9-16, 18-25, and 27-30.

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims canceled: 8, 17, and 26.
2. Claims withdrawn from consideration but not canceled: None.
3. Claims pending: 1-7, 9-16, 18-25, and 27-30.
4. Claims allowed: None.
5. Claims rejected: 1-3, 5-7, 9-12, 14-16, 18-21, 23-25, and 27-30.
6. Claims objected to: 4, 13, and 22.

C. CLAIMS ON APPEAL

The Claims on appeal are: 1-7, 9-16, 18-25, and 27-30.

STATUS OF AMENDMENTS

Amendments to claims 28-30 were submitted after the final office action of October 13, 2006. The Examiner entered the amendments as per the Advisory Action dated February 6, 2007.

SUMMARY OF CLAIMED SUBJECT MATTER

A. CLAIM 1 - INDEPENDENT

The subject matter of claim 1 is directed to a method in a data processing system for providing valid translation entries in a translation control entry table for all supported direct memory addresses (Specification, p. 1, ll. 9-13; and Figure 3). The method includes reserving a page in system memory to form a reserved page (Specification, p. 4, ll. 7-8; p. 13, ll. 1-9; and p. 16, ll. 14-15), writing the reserved page (Specification, p. 4, ll. 10-11; and p. 13, ll. 1-9), selecting a region in the system memory for the translation control entry table (Specification, p. 4, ll. 11-13; p. 11, ll. 19-20; and p. 16, ll. 15-17), and initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page (Specification, p. 4, ll. 13-20; p. 11, ll. 20-28; p. 12, l. 26 – p. 13, l. 20; and figure 4).

B. CLAIM 10 - INDEPENDENT

The subject matter of claim 10 is directed to a data processing system for providing valid translation entries in a translation control entry table for all supported direct memory addresses (Specification, p. 1, ll. 9-13; p. 6, l. 3 through p. 7, l. 17; p. 17, ll. 11-29; Figure 1; and Figure 3). The data processing system includes reserving means for reserving a page in system memory to form a reserved page (Specification, p. 4, ll. 7-8; p. 6, l. 3 through p. 7, l. 17; p. 13, ll. 1-9; p. 16, ll. 14-15; p. 17, ll. 11-29; and Figure 1), writing means for writing the reserved page (Specification, p. 4, ll. 7-8; p. 6, l. 3 through p. 7, l. 17; p. 13, ll. 1-9; p. 17, ll. 11-29; and Figure 1), selecting means for selecting a region in the system memory for the translation control entry table (Specification, p. 4, ll. 11-13; p. 6, l. 3 through p. 7, l. 17; p. 11, ll. 19-20; p. 13, ll. 10-11; p. 16, ll. 15-17; p. 17, ll. 11-29; and Figure 1), and initializing means for initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page (Specification, p. 4, ll. 13-20; p. 6, l. 3 through p. 7, l. 17; p. 11, ll. 20-28; p. 12, l. 26 – p. 13, l. 20; p. 17, ll. 11-29; Figure 1; and Figure 4).

C. CLAIM 11 - DEPENDENT

Claim 11 is directed to the data processing system of claim 10, further including updating means for updating an entry in the translation control entry table, wherein a physical memory page

replaces the reserved page when the entry is used by an operating system's device driver (Specification p. 6, l. 3 through p. 7, l. 17; p. 13, l. 21 – p. 14, l. 30; p. 17, ll. 11-29; Figure 1; and Figure 5.

D. CLAIM 12 - DEPENDENT

Claim 12 is directed to the data processing system of claim 11, further including restoring means for restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system (Specification p. 6, l. 3 through p. 7, l. 17; p. 17, ll. 5-29; and Figure 1).

E. CLAIM 19 - INDEPENDENT

The subject matter of claim 19 is directed to a computer program product in a recordable-type medium for providing valid translation entries in a translation control entry table for all supported direct memory addresses (Specification, p. 1, ll. 9-13; p. 6, l. 3 through p. 7, l. 17; p. 17, ll. 11-29; Figure 1; and Figure 3). The computer program product includes first instructions for reserving a page in system memory to form a reserved page (Specification, p. 4, ll. 7-8; p. 6, l. 3 through p. 7, l. 17; p. 13, ll. 1-9; p. 16, ll. 14-15; p. 17, ll. 11-29; and Figure 1), second instructions for writing the reserved page (Specification, p. 4, ll. 7-8; p. 6, l. 3 through p. 7, l. 17; p. 13, ll. 1-9; p. 17, ll. 11-29; and Figure 1), third instructions for selecting a region in the system memory for the translation control entry table (Specification, p. 4, ll. 11-13; p. 6, l. 3 through p. 7, l. 17; p. 11, ll. 19-20; p. 13, ll. 10-11; p. 16, ll. 15-17; p. 17, ll. 11-29; and Figure 1), and fourth instructions for initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page (Specification, p. 4, ll. 13-20; p. 6, l. 3 through p. 7, l. 17; p. 11, ll. 20-28; p. 12, l. 26 – p. 13, l. 20; p. 17, ll. 11-29; Figure 1; and Figure 4).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to review on appeal are as follows:

A. GROUND OF REJECTION 1 (Claims 1-3, 5, 6, 10-12, 14, 15, 19-21, 23, 24, and 28-30)

Whether claims 1-3, 5, 6, 10-12, 14, 15, 19-21, 23, 24, and 28-30 fail to be anticipated under 35 U.S.C. §102 by *Dawkins et al.*, Method and Apparatus to Power Off and/or Reboot Logical Partitions in a Data Processing System, U.S. Patent Application Publication 2002/0124194, March 1, 2001 (hereinafter "*Dawkins*").

B. GROUND OF REJECTION 2 (Claims 7, 16, and 25)

Whether the Examiner failed to state a *prima facie* obviousness rejection against claims 7, 16, and 25 under 35 U.S.C. §103(a) over *Dawkins* in view of *Tanenbaum et al.*, Operating Systems: Design and Implementation, 1997 (hereinafter "*Tanenbaum*").

C. GROUND OF REJECTION 3 (Claims 9, 18, and 27)

Whether the Examiner failed to state a *prima facie* obviousness rejection against claims 9, 18, and 27 under 35 U.S.C. §103(a) over *Dawkins*.

ARGUMENT

A. GROUND OF REJECTION 1 (Claims 1-3, 5, 6, 10-12, 14, 15, 19-21, 23, 24, and 28-30)

The first ground of rejection is whether claims 1-3, 5, 6, 10-12, 14, 15, 19-21, 23, 24, and 28-30 fail to be anticipated under 35 U.S.C. §102 by *Dawkins et al.*, Method and Apparatus to Power Off and/or Reboot Logical Partitions in a Data Processing System, U.S. Patent Application Publication 2002/0124194, March 1, 2001 (hereinafter "*Dawkins*"). This rejection is in error and should be reversed.

A.1. Claims 1, 5, 10, 14, 19, 23, and 28-30

A.1.i. Response to Rejection

Claim 1 is a representative claim in this grouping of claims. Claim 1 is as follows:

> 1. A method in a data processing system for providing valid translation entries in a translation control entry table for all supported direct memory addresses, comprising:
>
> reserving a page in system memory to form a reserved page;
>
> writing the reserved page;
>
> selecting a region in the system memory for the translation control entry table; and
>
> initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page.

A prior art reference anticipates the claimed invention under 35 U.S.C. §102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Regarding claim 1, the Examiner states that:

> Per claims 1, 10 and 19, Dawkins teaches a method in a data processing system for providing valid translation entries in a translation control entry table (TCE facility and TCE Table, see Pg. 4, Para. [0043], [0044], [0046]) for all supported direct memory addresses, comprising:

> reserving a page in system memory ("a reserved page per image ...", see Pg. 4, Para. [0046]) for form a reserved page (the reserved page clearly must be formed first before being pointed to);
>
> writing the reserved page (a page of memory is written to when a write operation from the operating systems addresses a memory range within the page);
>
> selecting a region in system memory for the translation control entry table (the TCE table must be stored somewhere in system memory for the Hypervisor and the operating systems to access it, see Pg. 4, Para. [0046]); and
>
> initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page ("initializes all entries in ... TCE table to point to a reserved page ... ", see Pg. 4, Para. [0044] and [0046]).

Final Office Action dated October 13, 2006, p. 3.

Dawkins does not anticipate claim 1 because *Dawkins* does not disclose all of the features of claim 1. Specifically, *Dawkins* fails to disclose (1) the feature of initializing all entries in the translation control entry table, (2) the feature wherein all entries are initialized to be valid in the feature of initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page, (3) the feature of selecting a region in the system memory for the translation control entry table, and (4) the feature of writing the reserved page.

A.1.i.a. *Dawkins* Fails to Disclose the Feature of Initializing all Entries in the Translation Control Entry Table

Dawkins fails to disclose the feature of initializing all entries in the translation control entry (TCE) table. The Examiner asserts otherwise, citing various portions of *Dawkins*. Each of these portions will be addressed in turn. The Examiner first cites the following portion of *Dawkins*:

> When an I/O operation starts on the bus, the TCE facility accesses the entry for that page in the TCE table, and uses the data in that entry as the most significant bits of the address to access memory, with the least significant bits being taken from the I/O address on the bus. The number of bits used from the bus is dependent on the size of the page, and is the number of bits necessary to address to the byte level within the page (e.g., for the 4 Kbyte page size example, the number of bits taken from the bus would be 12, as that is the number of bits required to address to the byte

> level within the 4 Kbyte page). Thus, the TCE provides bits to determine which page in memory is addressed, and the address bits taken from the I/O bus determines the address within the page.

Dawkins, paragraph 44.

Neither the cited portion nor any other portion of *Dawkins* discloses the feature of initializing all entries in the TCE table. *Dawkins* discloses a system for powering-off and rebooting logical partitions in a data processing system. *Dawkins* also discloses providing direct memory access (DMA) for each I/O adapter in the partitioned data processing system using a TCE facility. The cited portion of *Dawkins* discloses only the manner in which the TCE table and the I/O bus provide bits to access memory. For example, TCE bits determine which page in the memory is addressed, and the bits from the I/O bus determine the address within the page.

On the other hand, claim 1 recites the feature of initializing all entries in the TCE table. The cited portion of *Dawkins* differs from the claimed feature because the cited portion discloses only the manner in which the TCE table and the I/O bus use bits to access memory, but fails to disclose initializing any entries in the TCE table, let alone all entries in the TCE table. In fact, the cited portion does not address initialization of a TCE table at all because the cited portion discloses how an I/O bus accesses a particular address within a page, which is unrelated to initializing a TCE table.

Dawkins not only fails to disclose the feature of initializing all entries in the TCE table, but actually explicitly discloses otherwise, as shown in the following portion of *Dawkins*, which is cited by the Examiner as supposedly disclosing this claimed feature:

> When platform 400 is initialized, a disjoint range of I/O bus DMA addresses is assigned to each of I/O adapters 448-462 for the exclusive use of the respective one of I/O adapters 448-462 by hypervisor 410. Hypervisor 410 then configures the terminal bridge range register (not shown) facility to enforce this exclusive use. Hypervisor 410 then communicates this allocation to the owning one of OS images 402-408. Hypervisor also initializes all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image that is owned by the OS image that is allocated to that I/O adapter, such that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images 402-408.

Dawkins, paragraph 46.

The cited portion of *Dawkins* fails to disclose the feature of initializing all entries in the TCE table. Instead, the cited portion discloses that the hypervisor initializes all entries in a particular I/O adapter's **associated section** of the TCE table to point to a particular reserved page

per image that is owned by the OS image allocated to that I/O adapter. *Dawkins* then discloses that by doing so unauthorized access to memory by an I/O adapter will not create an error that could affect one of the other OS images.

In stark contrast, claim 1 requires initializing ***all*** entries in the TCE table. Again, *Dawkins* teaches only initializing all entries ***in a particular I/O adapter's associated section*** of the TCE table. Because these two features are different, the anticipation rejection is in error. *Dawkins* does not anticipate claim 1 for this reason alone.

Furthermore, *Dawkins*' failure to disclose initializing all entries in the TCE table is expected because initialization of the TCE table takes place in the context of *Dawkins*' partitioned data processing system. *Dawkins* implements a TCE table to provide direct memory access for each partition and its components, and treats each partition as a separate unit. For example, *Dawkins* discloses that "[t]he secure DMA window provides access from an I/O adapter to memory which is allocated to the same partition as the I/O adapter, while preventing the I/O adapter from getting access to the memory allocated to a different partition." *Dawkins*, paragraph 41. Hence, *Dawkins* fails to disclose, and has no reason to disclose, initializing all entries for a TCE table because *Dawkins* treats each partition as a separate unit with respect to direct memory access TCE mapping. Accordingly, *Dawkins* does not disclose all of the features of claim 1.

A.1.i.b. *Dawkins* Fails to Disclose the Feature Wherein all Entries are Initialized to be Valid in the Feature of Initializing all Entries in the Translation Control Entry Table, Wherein all Entries are Initialized to be Valid and Contain the Address of the Reserved Page

Dawkins also fails to disclose the feature wherein all entries are initialized to be valid in the feature of initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page. The Examiner asserts otherwise, citing paragraphs 44 and 46 of *Dawkins*, both of which have been reproduced above. Each of these portions will be addressed in turn.

Neither paragraph 44 nor any other portion of *Dawkins* discloses the feature wherein all entries are initialized to be valid. Paragraph 44 of *Dawkins* teaches only the manner in which the TCE table and the I/O bus provide bits to access memory. For example, TCE bits determine which page in the memory is addressed, and the bits from the I/O bus determine the address within the page.

In contrast, paragraph 44 of *Dawkins* fails to disclose the feature wherein all entries are initialized to be valid. The cited portion of *Dawkins* differs from the claimed feature because the cited portion discloses only the manner in which the TCE table and the I/O bus use bits to access memory, but fails to discloses initializing entries in a TCE table, let alone initializing all entries to be valid, as claimed. Because paragraph 44 does not relate to initializing a TCE table, paragraph 44 fails to disclose the feature wherein all entries are initialized to be valid.

The Examiner also alleges that paragraph 46 of *Dawkins* discloses the feature wherein all entries are initialized to be valid. Paragraph 46 has been reproduced above. Paragraph 46, however, discloses only a hypervisor that allocates bus DMA addresses for the exclusive use by the I/O adapters, and then communicates the allocation to the OS images. The hypervisor initializes all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image. Paragraph 46 of *Dawkins* differs from the claimed feature because paragraph 46 discloses only initializing entries of TCE table to point to a particular reserved page, but fails to disclose that the entry pointing to the reserved page is actually valid. Hence, a subsequent DMA translation may still result in an unrecoverable error because of an invalid entry in the TCE table. Thus, paragraph 46 fails to disclose the feature wherein all entries are initialized to be valid in the feature of initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page. Accordingly, *Dawkins* does not disclose all of the features of claim 1.

A.1.i.c. *Dawkins* Fails to Disclose the Feature of Selecting a Region in the System Memory for the Translation Control Entry Table

Dawkins also fails to disclose the feature of selecting a region in the system memory for the translation control entry table. The Examiner asserts otherwise, citing paragraph 46 of *Dawkins*, which has been reproduced above. However, neither paragraph 46 nor any other portion of *Dawkins* discloses the feature of selecting a region in the system memory for the translation control entry table. Paragraph 46 discloses only a hypervisor that assigns bus DMA addresses for the exclusive use by the I/O adapters, and then communicates this allocation to the OS images. Paragraph 46 does not relate to the storage of a TCE table on memory.

On the other hand, claim 1 recites the feature of selecting a region in the system memory for the translation control entry table. Nowhere does paragraph 46 disclose a region of memory for the TCE table. For example, in the only mention in paragraph 46 of a "TCE table," *Dawkins* states

that the "[h]ypervisor also initializes all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image that is owned by the OS image that is allocated to that I/O adapter, such that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images 402-408." However, the cited statement does not relate to, and says nothing about, the TCE table's location in memory, let alone disclose selecting a region in the system memory for the TCE table.

In the Final Office Action, the Examiner states that "the TCE table must be stored somewhere in system memory for the Hypervisor and the operating systems to access it." Final Office Action dated October 13, 2006, p. 3. However, just because "the TCE table must be stored somewhere," does not mean that *Dawkins* discloses selecting a region in system memory for the TCE table. *Dawkins* must disclose the claimed feature, but fails to do so, as shown above. Therefore, *Dawkins* fails to disclose the feature of selecting a region in the system memory for the translation control entry table. Accordingly, *Dawkins* does not disclose all of the features of claim 1.

A.1.i.d. *Dawkins* Fails to Disclose the Feature of Writing the Reserved Page

In addition, *Dawkins* fails to disclose the feature of writing the reserved page. The Examiner asserts otherwise, but fails to particularly point out any portion of *Dawkins* that discloses this feature. Instead, the Examiner states only that "a page of memory is written to when a write operation from the operating systems addresses a memory range within the page." Final Office Action dated October 13, 2006, p. 3. This assertion does not show how *Dawkins* discloses the claimed feature at issue. In fact, *Dawkins* does not anywhere actually disclose the feature of writing the reserved page, as recited in claim 1. For example, in the only mention in *Dawkins* of a "reserved page," *Dawkins* states that the "[h]ypervisor also initializes all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image that is owned by the OS image that is allocated to that I/O adapter, such that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images 402-408." *Dawkins*, paragraph 46. However, the cited statement only mentions a "reserved page," but says nothing about how the reserved page got there, such as by writing the reserved page, as claimed. Therefore, *Dawkins* does not disclose the feature of writing the reserved page. Accordingly, *Dawkins* does not anticipate claim 1 or the remaining claims in this grouping of claims.

A.1.ii. Rebuttal to Examiner's Responses

In response to the facts established above regarding the feature of initializing all entries in the translation control entry table, the Examiner asserts that:

> [I]t should be clear that each section of the TCE table for a particular I/O adapter can also be interpreted as a smaller TCE table for that particular I/O adapter only, since the Applicant admits that *Dawkins* can initialize all the entries in a section of the TCE table just for that particular I/O adapter. Since *Dawkins*' invention provides the means to distinguish the section's of the overall TCE table by the particular I/O adaptors the sections belong to, it is clear that the sections can all be considered as TCE tables for their respective I/O adaptors. Since the Applicant already admits that *Dawkins* initializes all entries of a section of the TCE table for a particular I/O adaptor, it is therefore concluded that Applicant's first argument is moot

Advisory Action dated February 6, 2007, p. 2.

The Examiner asserts that "it should be clear that each section of the TCE table for a particular 110 adapter can also be interpreted as a smaller TCE table for that particular 110 adapter only." However, *Dawkins* nowhere discloses that a particular I/O adapter's associated section of the TCE table is itself a TCE table, and the Examiner fails to cite any portion of *Dawkins* that discloses otherwise. For example, *Dawkins* states that "[w]hen an I/O operation starts on the bus, the TCE facility accesses the entry for that page in the TCE table, and uses the data in that entry as the most significant bits of the address to access memory, with the least significant bits being taken from the I/O address on the bus." *Dawkins*, paragraph 44. However, the cited statement does not disclose a "smaller TCE table" within the disclosed TCE table. On the contrary, the cited statement, as well as the remainder of *Dawkins*' disclosure, consistently refers to only one TCE table that applies to all I/O adapters. Returning to the portion of *Dawkins* cited by the Examiner, nowhere does paragraph 46 disclose initializing all entries for the only TCE table that *Dawkins* discloses. Instead, paragraph 46 discloses "initializing all entries in a particular I/O adapter's associated section of the TCE table," which is not the same as initializing all entries in the TCE table, as claimed.

The Examiner also asserts that "[s]ince *Dawkins*' invention provides the means to distinguish the section's of the overall TCE table by the particular I/O adaptors the sections belong to, it is clear that the sections can all be considered as TCE tables for their respective I/O adaptors." Advisory Action dated February 6, 2007, p. 2. However, just because *Dawkins* has the means to divide a TCE table into sections that are associated with respective I/O adapters, does not mean that *Dawkins* discloses that a section of a TCE table is itself a TCE table. In fact, *Dawkins*' provision of

means to divide a TCE table into sections associated with a particular I/O adapter reveals that *Dawkins* does not intend to associate each I/O adapter with a full TCE table. In other words, if *Dawkins* really did associate each I/O adapter with a TCE table and initialize all entries for that TCE table, as asserted by the Examiner, then *Dawkins* would not need "the means to distinguish the section's of the overall TCE table by the particular I/O adaptors the sections belong to." Advisory Action dated February 6, 2007, p. 2. Therefore, the Examiner's assertion further illustrates that *Dawkins* fails to disclose the feature of initializing all entries in the TCE table.

Also, because "initializing all entries in a particular I/O adapter's associated section of the TCE table," as disclosed in paragraph 46 of *Dawkins*, is not the same as initializing all entries in the TCE table, as claimed, the Examiner incorrectly concluded that Applicant's arguments are moot. As shown above, *Dawkins* discloses, and claim 1 recites, two different features, and therefore *Dawkins* fails to disclose all of the features of claim 1.

In response to the facts established above regarding the feature wherein all entries are initialized to be valid, the Examiner asserts that:

> The Applicant further states that Dawkins does not teach these limitations because Dawkins does not verify that the reserved page is actually valid (see Remarks, Pg.9, para.1). However, verifying the entries is not a claimed feature of the invention, and the independent claims merely recite "... all entries are initialized to be valid ...". The Examiner interpreted the claims without considering the specific detail described in the specification (see specification, pg. 11) about how the entries are initialized to be valid and rejected the claims accordingly. To one ordinarily skilled the art, the TCE entries initialized by Dawkins' hypersivor [sic] to point to a reserved page owned by an OS image in order to prevent errors caused by unauthorized accesses are considered to be valid (see Dawkins, pg.4, para. [0046]. The Applicant must recite the features in the claims in order for them to be considered. The Applicant also argued that the initialization step is not inherently anticipated by Dawkins because this step is not necessarily present (see Remarks, pg.10, para. 1), although the Examiner presented clear evidence that Dawkins explicitly, not inherently teaches this step as set forth in claims 1, 10 and 19's rejections. What is not necessarily present in the Applicant's admitted prior arts (see specification, pg.16, para.1) is clearly present in Dawkins' teaching.

Final Office Action dated October 13, 2006, p. 7.

The Examiner asserts that "verifying the entries is not a claimed feature" and that the Examiner ignored the detail in the specification with regard to how the entries are initialized to be valid. The Examiner incorrectly suggests that the Applicant relies upon the specification with

respect to the claimed feature at issue. As shown in Section A.1.i, *Dawkins* fails to disclose the feature wherein all entries are initialized to be valid. The description of this claimed feature in the specification is not at issue, only the plain meaning of the claimed term. Claim 1 requires that the entries are initialized to be valid. Instead, *Dawkins* discloses only that the entries are initialized to point to a particular reserved page per image, but discloses nothing about the validity of the TCE table entries. In fact, elsewhere in his rebuttal, the Examiner admits that "*Dawkins* does not teach how to indicate/mark an entry as valid." Final Office Action of October 13, 2006, p. 8. Therefore, *Dawkins* does not teach this claimed feature.

Nevertheless, the Examiner states that, "[t]o one ordinarily skilled the art, the TCE entries initialized by *Dawkins*' hypersivor [sic] to point to a reserved page owned by an OS image in order to prevent errors caused by unauthorized accesses are considered to be valid." Final Office Action of October 13, 2006, p. 7. Thus, the Examiner appears to assert that *Dawkins* teaches initializing all entries in the TCE to be valid, as in claim 1, because *Dawkins* teaches initializing TCE entries to prevent errors.

However, this interpretation of *Dawkins* is clearly in error. *Dawkins* specifically states that the entries are initialized, "such that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images." Thus, *Dawkins* teaches that errors caused by unauthorized access are prevented – not that all errors are prevented and not that all entries are initialized to be valid, as in claim 1. Thus, again, *Dawkins* does not anticipate claim 1.

Nonetheless, the Examiner further asserts that:

> [T]he Applicant is respectfuly [sic] reminded that TCE entry data that points to a particular reserved page is valid data in view of the plain meaning of the term "valid". Assigning/initializing an entry to point to a particular reserved page is a valid assignment with valid data values. Therefore *Dawkins* does not inherently teach the above stated claim limitation as suggested by the Applicant, but does so explicitly by teaching that the entries are initialized to point to a particular reserved page. The issue of whether *Dawkins* teaches that all errors are prevented is not relevant to the claims under discussion.

Advisory Action dated February 6, 2007, p. 2.

The Examiner asserts that "[a]ssigning/initializing an entry to point to a particular reserved page is a valid assignment with valid data values." However, the Examiner again fails to cite any portion of *Dawkins* that relates to the validity of TCE table entries. Instead, the Examiner inserts

the word "valid" in front of the words "assignment" and "data values" and concludes that *Dawkins* must now disclose the claimed feature. However, *Dawkins* does not mention the word "valid" anywhere in its disclosure, let alone disclose initializing all entries to be valid. *Dawkins* also does not teach an equivalent word. Instead, *Dawkins* teaches that the entries are initialized to point to a particular reserved page per image. Because these features are not equivalent, *Dawkins* does not anticipate claim 1.

The Examiner also states that "[t]he issue of whether *Dawkins* teaches that all errors are prevented is not relevant to the claims under discussion." However, Applicants only addressed the issue of error prevention to rebut the Examiner's erroneous assertion that "[t]o one ordinarily skilled the art, the TCE entries initialized by *Dawkins*' hypersivor [sic] to point to a reserved page owned by an OS image in order to prevent errors caused by unauthorized accesses are considered to be valid." Final Office Action of October 13, 2006, p. 7. Because *Dawkins* fails to disclose the feature wherein all entries are initialized to be valid, *Dawkins* does not disclose all of the features of claim 1.

In response to the facts established above regarding the feature of writing the reserved page, the Examiner asserts that:

> As for the argument that *Dawkins* does not teach "writing the reserved page", it should be clear that *Dawkins*' reserved page is owned and accessed by an OS image and an I/O adapter for DMA operations, and the page must be written (see *Dawkins*, pg.4, para.[0046]-[0047]) as memory operations include write operations (data read from the page must be written into the page first).

Final Office Action dated October 13, 2006, pp. 7-8.

In his response, the Examiner cites paragraphs 46 and 47 of *Dawkins* in his assertion that the reserved page "must be written." Each paragraph will be addressed in turn. Paragraph 46 has been reproduced above. Neither paragraph 46 nor any other portion of *Dawkins* discloses the feature of writing the reserved page. Paragraph 46 discloses only a hypervisor that assigns bus DMA addresses for the exclusive use by the I/O adapters, and then communicates this allocation to the OS images. The only portion of paragraph 46 that mentions a "reserved page" states that the "[h]ypervisor also initializes all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image that is owned by the OS image that is allocated to that I/O adapter, such that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images 402-408." However, the cited statement discloses

nothing about writing a reserved page, and instead discloses only initializing entries of a section of a TCE table to point to a reserved page. Hence, paragraph 46 does not disclose the claimed feature.

Nonetheless, the Examiner cites the following paragraph of *Dawkins*:

> When an owning one of OS images 402-408 requests to map some of its memory for a DMA operation, it makes a call to the hypervisor 410 including parameters indicating the I/O adapter, the memory address range, and the associated I/O bus DMA address range to be mapped. The hypervisor 410 checks that the I/O adapter and the memory address range are allocated to the owning one of OS images 402-408. The hypervisor 410 also checks that the I/O bus DMA range is within the range allocated to the I/O adapter. If these checks are passed, the hypervisor 410 performs the requested TCE mapping. If these checks are not passed, the hypervisor rejects the request.

Dawkins, paragraph 47.

However, the cited paragraph does not disclose a reserved page at all, let alone writing a reserved page. Instead, the cited paragraph discloses an OS image request to map some of its memory for a DMA operation. The cited paragraph also discloses that the hypervisor performs a series of checks to ensure that the mapping request involves entities that are allocated to one another. No reserved page is disclosed in paragraph 47. Therefore, paragraph 47 does not disclose writing the reserved page.

The Examiner also asserts that "the page must be written ... as memory operations include write operations (data read from the page must be written into the page first)." Final Office Action of October 13, 2006, p. 8. However, whether memory operations include write operations does not relate to whether *Dawkins* discloses writing the reserved page. Even if memory operations do include write operations, then *Dawkins* must still disclose the claimed feature. Also, *Dawkins* nowhere discloses that data is "read from the page," but instead discloses only initializing entries of a section of a TCE table to point to a reserved page. However, even assuming, *arguendo*, that *Dawkins* does disclose reading from a reserved page, reading from a reserved page is not the same as writing a reserved page. Hence, *Dawkins* fails to disclose the feature of writing a reserved page.

Applicants have demonstrated that *Dawkins* does not disclose the features of claim 1. Similarly, Applicants have demonstrated that the Examiner's assertions and response regarding the

teachings of *Dawkins vis-à-vis* claim 1 are incorrect. Therefore, *Dawkins* does not anticipate claim 1 or any other claim in this grouping of claims. Accordingly, Applicants request that the Board of Patent Appeals and Interferences overturn the rejection and direct the Examiner to allow the claims.

A.2. Claims 2, 11, and 20

Claim 2 is a representative claim in this grouping of claims. Claim 2 is as follows:

> 2. The method of claim 1, further comprising:
> updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver.

Regarding claim 2, that Examiner states that:

> Per claims 2, 11 and 20, Dawkins further teaches updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver (TCE mapping with 110 adapter DMA range, see Pg. 4, Para. [0047] and [0048]).

Final Office Action dated October 13, 2006, p. 4.

Claim 2 depends from claim 1. As shown above, *Dawkins* does not anticipate claim 1. Therefore, *Dawkins* does not anticipate claim 2 at least by virtue of its dependency on claim 1. Additionally, claim 2 claims other additional combinations of features not disclosed by *Dawkins*.

Dawkins fails to disclose the feature of updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver. The Examiner asserts otherwise, citing various portions of *Dawkins*. Each of these portions will be addressed in turn. Applicants first address the following portion of *Dawkins*:

> When an owning one of OS images 402-408 requests to map some of its memory for a DMA operation, it makes a call to the hypervisor 410 including parameters indicating the I/O adapter, the memory address range, and the associated I/O bus DMA address range to be mapped. The hypervisor 410 checks that the I/O adapter and the memory address range are allocated to the owning one of OS images 402-408. The hypervisor 410 also checks that the I/O bus DMA range is within the range allocated to the I/O adapter. If these checks are passed, the hypervisor 410 performs the requested TCE mapping. If these checks are not passed, the hypervisor rejects the request.

Dawkins, paragraph 47.

Neither the cited portion nor any other portion of *Dawkins* discloses the feature of updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver. Instead, the cited paragraph discloses an OS image request to map some of its memory for a DMA operation. The cited paragraph also discloses that the hypervisor performs a series of checks to ensure that the mapping request involves entities that are allocated to one another. However, the cited paragraph does not relate to updating entries in a TCE table, let alone replacing the reserved page with a physical memory page when TCE table entry is used by an operating system's device driver.

For example, the cited paragraph contains the following statement, which contains the paragraph's only reference to a "TCE": "If these checks are passed, the hypervisor 410 performs the requested TCE mapping. If these checks are not passed, the hypervisor rejects the request." *Dawkins*, paragraph 47. However, the cited statement discloses only that the hypervisor performs the requested TCE mapping, but nowhere discloses updating an entry in the TCE table, as claimed. Furthermore, the cited statement nowhere discloses replacing the reserved page with a physical memory page when TCE table entry is used by an operating system's device driver. Neither the cited statement nor paragraph 47 makes any reference to a reserved page at all. Hence, paragraph fails to disclose the feature of updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver.

Next, the Examiner cites the following paragraph of *Dawkins* against claim 2:

> Hypervisor 410 also may provide the OS images 402-408 running in multiple logical partitions each a virtual copy of a console and operator panel. The interface to the console is changed from an asynchronous teletype port device driver, as in the prior art, to a set of hypervisor firmware calls that emulate a port device driver. The hypervisor 410 encapsulates the data from the various OS images onto a message stream that is transferred to a terminal, such as hardware system console computer 480. In these examples, multiple hardware system consoles are supported. As illustrated, hardware system console 482 and hardware system console 484 also are present.

Dawkins, paragraph 48.

However, the cited portion does not relate to TCE mapping, let alone disclose the feature of updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver. Instead, the cited paragraph discloses that a hypervisor may provide each OS image a virtual copy of a console and

operator panel. The cited paragraph nowhere discloses a TCE table, TCE mapping, direct memory access, or a reserved page, and does not relate to the claimed feature. Consequently, the cited paragraph does not disclose updating TCE table entries, or replacing the reserved page with a physical memory page when a TCE table entry is used by an operating system's device driver. Therefore, *Dawkins* fails to disclose the feature of updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver.

Applicants have demonstrated that *Dawkins* does not disclose the features of claim 2. Similarly, Applicants have demonstrated that the Examiner's assertions regarding the teachings of *Dawkins vis-à-vis* claim 2 are incorrect. Therefore, *Dawkins* does not anticipate claim 2 or any other claim in this grouping of claims. Accordingly, Applicants request that the Board of Patent Appeals and Interferences overturn the rejection and direct the Examiner to allow the claims.

A.3. Claims 3, 12, and 21

Claim 3 is a representative claim in this grouping of claims. Claim 3 is as follows:

> 3. The method of claim 2, further comprising:
> restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system.

Regarding claim 3, the Examiner states that:

> Per claims 3, 12 and 21, *Dawkins* further teaches restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system (reserving the page is done during platform initialization, at which point the previous mapping by an operating system must be replaced by the page reservation, see Pg. 4, Para. [0046]).

Final Office Action dated October 13, 2006, p. 4.

Claim 3 depends from claim 2, which depends from claim 1. As shown above, *Dawkins* does not anticipate claims 1 or 2. Therefore, *Dawkins* does not anticipate claim 3 at least by virtue of its dependency claim 2, which depends on claim 1. Additionally, claim 3 claims other additional combinations of features not disclosed by *Dawkins*.

Dawkins fails to disclose the feature of restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system. The Examiner asserts otherwise, citing the following paragraph of *Dawkins*:

> When platform 400 is initialized, a disjoint range of I/O bus DMA addresses is assigned to each of I/O adapters 448-462 for the exclusive use of the respective one of I/O adapters 448-462 by hypervisor 410. Hypervisor 410 then configures the terminal bridge range register (not shown) facility to enforce this exclusive use. Hypervisor 410 then communicates this allocation to the owning one of OS images 402-408. Hypervisor also initializes all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image that is owned by the OS image that is allocated to that I/O adapter, such that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images 402-408.

Dawkins, paragraph 46.

Neither the cited paragraph nor any other portion of *Dawkins* discloses the feature of restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system. Paragraph 46 discloses only a hypervisor that allocates bus DMA addresses for the exclusive use by the I/O adapters, and then communicates the allocation to the OS images. Paragraph 46 also discloses that the hypervisor initializes all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image. However, initializing all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image is not the same as restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system.

On the other hand, claim 3 recites the feature of restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system. *Dawkins*' disclosure differs from the claimed feature because even assuming, *arguendo*, that initializing all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image teaches the claimed feature of restoring the entry in the translation control entry table with the reserved page, *Dawkins* still fails to disclose the claimed condition of "when the entry is no longer used by an operating system." Instead, *Dawkins* discloses initializing all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image regardless of whether the entry is being used by an operating system.

For example, paragraph 46 states that the "[h]ypervisor also initializes all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image that is owned by the OS image that is allocated to that I/O adapter, such that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images 402-408." However, the cited statement nowhere discloses when the entry initialization occurs, let

alone when an entry is no longer used by an operating system, as claimed. Instead, the cited statement discloses a result of the initialization when its states "such that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images." However, the cited result does not relate to when the entry initialization occurs. Because neither the cited paragraph nor any other portion of *Dawkins* discloses when the initialization occurs, *Dawkins* fails to disclose the feature of restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system.

Applicants have demonstrated that *Dawkins* does not disclose the features of claim 3. Similarly, Applicants have demonstrated that the Examiner's assertions regarding the teachings of *Dawkins vis-à-vis* claim 3 are incorrect. Therefore, *Dawkins* does not anticipate claim 3 or any other claim in this grouping of claims. Accordingly, Applicants request that the Board of Patent Appeals and Interferences overturn the rejection and direct the Examiner to allow the claims.

A.4. Claims 6, 15, and 24

Claim 6 is a representative claim in this grouping of claims. Claim 6 is as follows:

> 6. The method of claim 1, wherein writing the reserved page includes setting all bytes within the reserved page to 0xFF.

Regarding claim 6, the Examiner states that:

> Per claims 6, 15 and 24, *Dawkins* further teaches writing the reserved page includes setting all bytes within the reserved page to 0xFF (reserving a page implies initializing the page, therefore the byte values within the reserved page are arbitrarily set to known values. Setting all bytes to 0xFF is merely a design choice).

Final Office Action dated October 13, 2006, p. 4.

Claim 6 depends from claim 1. As shown above, *Dawkins* does not anticipate claim 1. Therefore, *Dawkins* dose not anticipate claim 6 at least by virtue of its dependency of claim 1. Additionally, claim 6 claims other additional combinations of features not disclosed by *Dawkins*.

Dawkins fails to disclose the feature wherein writing the reserved page includes setting all bytes within the reserved page to 0xFF. The Examiner fails to cite any portion of *Dawkins* with respect to this claimed feature.

As an initial matter, *Dawkins* does not disclose the feature wherein writing the reserved page includes setting all bytes within the reserved page to 0xFF because *Dawkins* fails to disclose the feature of writing the reserved page, as claimed in claim 1. As shown in Section A.1, *Dawkins*

fails to disclose the feature of writing the reserved page, as claimed in claim 1. Therefore, *Dawkins* also fails to disclose the feature wherein writing the reserved page includes setting all bytes within the reserved page to 0xFF.

As a second matter, even assuming, *arguendo*, that *Dawkins* does disclose writing the reserved page, *Dawkins* still fails to disclose the feature wherein writing the reserved page includes setting all bytes within the reserved page to 0xFF. *Dawkins* nowhere discloses setting any bytes to the value of "0xFF," let alone setting all bytes within the reserved page to 0xFF. Where *Dawkins* does disclose setting bytes to a particular value, the bytes do not relate to a reserved page, and the bytes are not set to 0xFF.

For example, *Dawkins* states that "[t]he service processor updates NVRAM processor table and the target address is set to 0xB00 for all processors of the partition." *Dawkins*, paragraph 67. However, the cited statement does not disclose setting any values to 0xFF, as claimed. Furthermore, the cited statement does not disclose, and does not relate to, a reserved page. Instead, the cited statement relates to setting the values for a NVRAM processor table, which is not the same as a reserved page because a NVRAM processor table contains addresses to which processors will look after being reset, while a reserved page is used in conjunction with a TCE table to facilitate direct memory access. Hence, *Dawkins* fails to disclose the feature wherein writing the reserved page includes setting all bytes within the reserved page to 0xFF.

Furthermore, the Examiner's assertion that "[s]etting all bytes to 0xFF is merely a design choice" is irrelevant to the issue of whether *Dawkins* discloses the claimed feature. Under 35 U.S.C. § 102, *Dawkins* must disclose the claimed feature either explicitly or inherently. As shown above, *Dawkins* fails to disclose the claimed feature, and the Examiner fails to prove otherwise.

Applicants have demonstrated that *Dawkins* does not disclose the features of claim 6. Similarly, Applicants have demonstrated that the Examiner's assertions regarding the teachings of *Dawkins* vis-à-vis claim 6 are incorrect. Therefore, *Dawkins* does not anticipate claim 6 or any other claim in this grouping of claims. Accordingly, Applicants request that the Board of Patent Appeals and Interferences overturn the rejection and direct the Examiner to allow the claims.

B. GROUND OF REJECTION 2 (Claims 7, 16, and 25)

The second ground of rejection is whether the Examiner failed to state a *prima facie* obviousness rejection against claims 7, 16, and 25 under 35 U.S.C. §103(a) over *Dawkins* in view of *Tanenbaum et al.*, Operating Systems: Design and Implementation, 1997 (hereinafter "*Tanenbaum*"). This rejection is in error and should therefore be overturned.

Claim 7 is a representative claim in this grouping of claims. Claim 7 is as follows:

> 7. The method of claim 1, wherein initializing all entries to be valid includes setting all valid bits to "1".

Regarding claim 7, the Examiner states that:

> Per claims 7, 16 and 25, *Dawkins* does not specifically teach setting all valid bits to "1". However, *Tanenbaum* teaches an address translation mechanism (TLB, see *Tanenbaum*, Pg. 328, Fig. 4-12) that sets valid bits of its table entries to "1" to indicate the entries are valid (in use, see Pg. 328, Ln. 20-21). Since *Dawkins* initializes its TCE table entries to contain the address of the reserved page as described in claim 1, the entries are in use and therefore valid. Hence, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to associate valid bits to the table entries and set the bits to "1" to indicate that the entries are valid (in use).

Final Office Action dated October 13, 2006, p. 5.

Applicants first respond to the rejection by showing that the proposed combination, when considered as a whole, does not teach or suggest all of the features of claim 7, and that the Examiner failed to state a proper teaching, motivation, or suggestion to combine the references. Applicants then refute the Examiner's response in the final office action of October 13, 2006.

B.1. Response to Rejection

B.1.i. The Proposed Combination Does Not Teach or Suggest All of the Features of Claim 7

If the Patent Office does not produce a *prima facie* case of unpatentability, then without more Applicants are entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985). A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994).

The Examiner failed to state a *prima facie* obviousness against claim 7 because the proposed combination, when considered as a whole, does not teach or suggest all of the features of claim 7. As shown in Section A.1., *Dawkins* does not teach all of the claimed features of independent claim 1, from which claim 7 depends. Additionally, *Dawkins* does not teach, suggest, or give any incentive to make the needed changes to reach claim 1. Absent the Examiner pointing out some teaching or incentive to implement *Dawkins* and the features of claim 1 distinguished in Section A.1., one of ordinary skill in the art would not be led to modify *Dawkins* to reach the present invention when the reference is examined as a whole.

Moreover, *Tanenbaum* fails to cure the deficiencies of *Dawkins* because *Tanenbaum* does not teach or suggest any of the features of claim 1. The Examiner does not assert otherwise. Instead, *Tanenbaum* teaches equipping computers with a small hardware device for mapping virtual addresses to physical addresses without going through the page table, which is wholly unrelated to these claimed features.

Because neither *Dawkins* nor *Tanenbaum* teach or suggest all of the features of claim 1, the proposed combination of *Dawkins* and *Tanenbaum*, when considered as a whole, does not teach or suggest all of the features of claim 7, which depends from claim 1. Therefore, under the standards of *In re Lowry* and *In re Grabiak*, the Examiner failed to state a *prima facie* obviousness rejection of claim 7 or any other claim in this grouping of claims.

B.1.ii. The Examiner has not Stated a Proper Teaching, Suggestion, or Motivation to Combine the References

B.1.ii.a. No Motivation Exists to Combine the References

A *prima facie* obviousness rejection against claim 7 has not been made because no proper teaching or suggestion to combine the references has been stated. A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). A proper *prima facie* case of obviousness cannot be established by combining the teachings of the prior art absent some teaching, incentive, or suggestion supporting the combination. *In re Napier*, 55 F.3d 610, 613, 34 U.S.P.Q.2d 1782, 1784 (Fed.

Cir. 1995); *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d 1566, 1568 (Fed. Cir. 1990). No such teaching or suggestion is present in the cited references and the Examiner has not pointed out any proper teaching or suggestion that is based on the prior art.

The Examiner cites the following portion of *Tanenbaum* in support of the above-referenced rejection: "Another bit indicates whether the entry is valid (i.e., in use) or not." *Tanenbaum*, p. 328, lines 20-21. As an initial matter, the cited portion of *Tanenbaum* provides no teaching, motivation, or suggestion to combine the references. Specifically, the cited portion does not suggest combining *Dawkins*' initialization of an I/O adapter's associated section of a TCE table with *Tanenbaum*'s indication of whether an entry is valid. Thus, the Examiner has not actually stated a teaching, motivation, or suggestion based on the references to combine the references.

As a second matter, given the teachings of each reference, one of ordinary skill in the art would be motivated to avoid combining the references. *Tanenbaum*, when viewed as a whole, sets forth a solution "to equip computers with a small hardware device for mapping virtual addresses to physical addresses without going through the page table." *Tanenbaum*, p.328, lines 11-13. The small hardware device eliminates the need for page tables that are kept in memory. *See*, *Tanenbaum*, p.327, line 28 – p.328, line 10. In stark contrast, *Dawkins* teaches that memory is mapped for a DMA operation by means of a TCE page table stored in the memory. *See*, *Dawkins*, paragraphs 43-46. Thus, in view of *Tanenbaum's* teaching, one of ordinary skill would be motivated to avoid combining the small hardware device of *Tanenbaum* with *Dawkins* because *Dawkins* creates the very problem that *Tanenbaum* seeks to eliminate.

Further, *Dawkins* teaches that the DMA mapping is performed by means of a TCE page table stored in system memory. Thus, *Dawkins* would have no need for *Tanenbaum's* extraneous hardware device to accomplish the DMA mapping that *Dawkins* teaches by means of the page table stored in memory. For this reason, one of ordinary skill in the art would be motivated against combining *Dawkins* and *Tanenbaum*.

Given that one of ordinary skill would be motivated against combining the references and given that no need exists to combine the references, no pre-existing teaching, suggestion, or motivation to combine the references exists. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against claim 7.

B.1.ii.b. One of Ordinary Skill in the Art Would Not Combine the References Because the References are Directed to Solving Different Problems

One of ordinary skill would not combine the references to achieve the invention of claim 7 because the references are directed towards solving different problems. It is necessary to consider the reality of the circumstances--in other words, common sense--in deciding in which fields a person of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor. *In re Oetiker*, 977 F.2d 1443 (Fed. Cir. 1992); *In re Wood*, 599 F.2d 1032, 1036, 202 U.S.P.Q. 171, 174 (CCPA 1979). In the case at hand, the cited references address distinct problems. Thus, no common sense reason exists to establish that one of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor. Accordingly, no teaching, suggestion, or motivation exists to combine the references and the Examiner has failed to state a *prima facie* obviousness rejection of claim 7.

Tanenbaum is directed to the problem of increasing the execution speed of paging schemes by equipping computers with a small hardware device, called a Translation Lookaside Buffer, for mapping virtual addresses to physical addresses without going through the page table. For example, *Tanenbaum* provides that:

> In most paging schemes, the page tables are kept in memory, due to their large size. Potentially, this design has an enormous impact on performance. Consider, for example, an instruction that copies one register to another. In the absence of paging, this instruction makes only one memory reference, to fetch the instruction. With paging, additional memory references will be needed to access the page table. Since execution speed is generally limited by the rate the CPU can get instructions and data out of the memory, having to make two page table references per memory reference reduces performance by 2/3. Under these conditions, on one would use it.
>
> ....
>
> The solution that has been devised is to equip computers with a small hardware device for mapping virtual addresses to physical addresses without going through the page table.

Tanenbaum, page 327, line 28 – page 328, line 13.

In stark contrast, *Dawkins* is directed to solving the problem of turning power on and off in a partitioned data processing system. For example, *Dawkins* provides that:

> The configuration of these different partitions are typically managed through a terminal, such as a hardware system console (HSC). These terminals use objects, also referred to as profiles that are defined and modified in HSC. The profiles are used to configure LPARs within the

> data processing system. Multiple HSCs may be present and used for maintaining and configuring LPARs in the data processing system. These profiles used to configure the data processing system in LPARs are often required to be accessible to any HSC that is in communication with the data processing system. Maintaining profiles between these HSCs are often difficult and require processes for maintaining synchronization of the profiles at each HSC. Therefore, it would be advantageous to have improved method, apparatus, and computer implemented instructions for maintaining profiles for different HSCs.
>
> With multiple partitions executing at the same time, a command to reset the data processing system will reset all the partitions. Similarly, pressing a reset button on the data processing system also will cause all of the partitions to reset. Further, turning off the power to the system may result in errors if all of the logical partitions have not been properly shut down. With these situations, the physical buttons for power and reset on a computer should not be used in a system using logical partitions.
>
> Therefore, it would be advantageous to have an improved method and apparatus for resetting and/or turning off power to a data processing system..

Dawkins, paragraphs 6-8.

Based on the plain disclosures of the references themselves, the references address completely distinct problems that are unrelated to each other. The problem of increasing the execution speed of paging schemes by equipping computers with a small hardware device, called a Translation Lookaside Buffer, for mapping virtual addresses to physical addresses without going through the page table is completely distinct from the problem of turning power on and off in a partitioned data processing system. Because the references address completely distinct problems, one of ordinary skill would have no reason to combine or otherwise modify the references to achieve the claimed invention. Thus, one of ordinary skill in the art would not combine these references to achieve the claimed inventions because no teaching, suggestion, or motivation exists to combine the references in the manner suggested by the Examiner. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against the claims.

B.1.ii.c. The Examiner Must Have Used Impermissible Hindsight When Fashioning the Rejections

In addition, the Examiner failed to state a *prima facie* obviousness rejection against the claims because the Examiner used impermissible hindsight when fashioning the rejection. Personal opinion cannot be substituted for what the prior art teaches because a *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject

matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). Additionally, "[i]t is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." *In re Hedges*, 228 U.S.P.Q. 685, 687 (Fed. Cir. 1986).

As shown above, one of ordinary skill would be motivated against combining the references and no need exists to combine the references. Also, the references address starkly different problems. Therefore, the Examiner could only have fashioned the rejections by using the Examiner's personal opinion or by picking and choosing features from starkly different references. The rejection appears to be based on "keyword searches" and the establishment of the existence of terms, rather than on a fair evaluation of the teachings of the references as a whole. Accordingly, the Examiner must have used impermissible hindsight when fashioning the rejections. Accordingly, under the standards of *In re Bell* and *In re Hedges*, the Examiner failed to state a *prima facie* obviousness rejection of the claims.

Based on the plain disclosures in the references, the only suggestion to modify the references is found in Applicants' specification. Hence, the Examiner must have used Applicants' specification to find a teaching, suggestion, or motivation to combine the references. Combining the references in this manner constitutes impermissible hindsight and fails to comport with the standards of *Graham v. John Deere Co.*, 383 U.S. 1 (1966), which requires a proper teaching, suggestion, or motivation to combine or modify references to achieve a proper obviousness rejection. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against claim 7.

B.2. Rebuttal to Examiner's Response

In response to the facts established above, the Examiner asserts:

> Regarding the Applicant's third argument (see Remarks, pg.14-15, section VI.B), the Applicant argued that *Dawkins* and *Tanenbaum* cannot be combined because they are directed to distinct problems. However, *Dawkins* already describes initializing entries TCE table. *Dawkins* does not teach how to indicate/mark an entry as valid, but it clearly indicates a motivation for a method to determine the status of the entries. *Tanenbaum*'s teaching, although not in the exact same topic as *Dawkins*', offers a well-known method of marking entries with "0" and "1" bits to indicate their status. Such a teaching does not deviate from the field of digital logic design, which is an area related to *Dawkins*' step of

> initializing TCE table entries. Determining how to initialize TCE table entries and initialize page table entries both direct to the problem of how to digitally mark a data table entry using binary values in a digital computing system. There is clearly sufficient motivation for the combination of *Dawkins* and *Tanenbaum*.

Final Office Action dated October 13, 2006, pp. 8-9.

The crux of the Examiner's response is that the references are both directed towards the field of digital logic design. For this reason, the Examiner believes that the references are related to the same problem and that the references are related to claim 7.

However, the Examiner's interpretation of the references is overly broad. Using the same reasoning provided by the Examiner, any set of references regarding digital logic design could be potentially combined and used in an obviousness rejection against claim 7. However, this belief does not comport with the standards of *Ex parte Clapp*, which requires that the Examiner provide a specific benefit or reason to combine the references to achieve the invention of claim 7. Instead, because of the standard in *Ex parte Clapp*, the Examiner must look to the exact teachings of the references to see whether the references address the same problems *within the field of digital logic design*.

In the case at hand, as shown above, the references to not address the same problems within the field of digital logic design. *Tanenbaum* addresses the problem of increasing the execution speed of paging schemes by equipping computers with a small hardware device, called a Translation Lookaside Buffer, for mapping virtual addresses to physical addresses without going through the page table. *Dawkins* addresses the problem of turning power on and off in a partitioned data processing system. Within the field of digital logic design, these problems are unrelated to each other. Therefore, one of ordinary skill in the art of digital logic design would not have a reason, teaching, suggestion, or motivation to combine the references to achieve the invention of claim 7.

The Examiner also states that "[d]etermining how to initialize TCE table entries and initialize page table entries both direct to the problem of how to digitally mark a data table entry using binary values in a digital computing system." Final Office Action of October 13, 2006, p. 9. However, *Dawkins* as nothing to do with the "problem of how to digitally mark a data table entry using binary values in a digital computing system," because *Dawkins* nowhere discloses digitally marking a data table entry table using a binary value, and the Examiner fails to cite any

portion of *Dawkins* that shows otherwise. Accordingly, the Examiner failed to state a *prima facie* obviousness rejection against claim 7 and against the other claims in this grouping of claims.

Applicants note that the issue of whether the references are directed towards different problems is distinct from the question of whether either *Dawkins* or *Tanenbaum* are non-analogous art to the claims. As stated above, the primary consideration here is that no teaching, suggestion, or motivation to combine the references exists because the references address different problems, not whether *Dawkins* or *Tanenbaum* are non-analogous art to the claims.

C. GROUND OF REJECTION 3 (Claims 9, 18, and 27)

The third ground of rejection is whether the Examiner failed to state a *prima facie* obviousness rejection against claims 9, 18, and 27 under 35 U.S.C. §103(a) over *Dawkins*. This rejection is in error and should be reversed.

Claim 9 is a representative claim in this grouping of claims. Claim 9 is as follows:

> 9. The method of claim 1, wherein the translation control entry table comprises a 2MB Translation Control Entry table having 512K 4-byte entries.

Regarding claim 9, the Examiner states:

> Per claims 9, 18 and 27, *Dawkins* does not specifically teach the size of the TCE table, the number of table entries, or the size of the table entries. However, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that these specific values are dictated by design choices and system parameters such as the size of system memory, page size, addressing format and performance costs.

Final Office Action dated October 13, 2006, p. 6.

The Examiner failed to state a *prima facie* obviousness against claim 9 because the proposed combination, when considered as a whole, does not teach or suggest all of the features of claim 9. As shown in Section A.1, *Dawkins* does not teach all of the claimed features of claim 1. Therefore, *Dawkins* fails to teach all of the claim features of claim 9, at least by virtue of its dependency on claim 1. Additionally, *Dawkins* does not teach, suggest, or give any incentive to make the needed changes to reach claim 9. Absent the Examiner pointing out some teaching or incentive to implement *Dawkins* and the features distinguished in Section A.1., one of ordinary skill in the art would not be led to modify *Dawkins* to reach the present invention when the reference is examined as a whole.

In addition, *Dawkins* does not teach or suggest the feature wherein the translation control entry table comprises a 2MB TCE table having 512K 4-byte entries as recited in claim 9. On the contrary, *Dawkins* nowhere teaches or suggests a size for the TCE table, let alone a 2MB TCE table having 512K 4-byte entries. At best, *Dawkins* discloses a size for a page, which is different from a TCE table. For example, *Dawkins* discloses that "[f]or IBM PowerPC processor based platforms, this size is generally 4 Kbytes per page." *Dawkins*, paragraph 43. However, the cited statement refers only to the size of a page, and not a TCE table. Thus, *Dawkins* fails to teach or suggest the feature wherein the translation control entry table comprises a 2MB TCE table having 512K 4-byte entries.

The Examiner states only that "design choice" and "system parameters" would render obvious the TCE table size and TCE table entry size recited in claim 9. However, "design choice" and "system parameters" appear to be offered as a substitute for a proper teaching, suggestion, or motivation to modify the reference. Such outdated maxims are improper substitutes for a proper teaching, suggestion, or motivation to modify or combine references under the mandated test for patentability set forth in *Graham v. John Deere Co.*, 383 U.S. 1 (1966). Accordingly, the proposed modification of *Dawkins* does not teach or suggest all of the features of claim 9 or any other claim in this grouping of claims.

D. CONCLUSION

As shown above, *Dawkins* does not anticipate the claims and the Examiner failed to state a *prima facie* obviousness rejection against any of the claims. Therefore, Applicants request that the Board of Patent Appeals and Interferences reverse the rejections. Additionally, Applicants request that the Board direct the Examiner to allow the claims.

/Theodore D. Fay III/
Theodore D. Fay III
Reg. No. 48,504
YEE & ASSOCIATES, P.C.
PO Box 802333
Dallas, TX 75380
(972) 385-8777

TF/KA

CLAIMS APPENDIX

The text of the claims involved in the appeal is as follows:

1. A method in a data processing system for providing valid translation entries in a translation control entry table for all supported direct memory addresses, comprising:

reserving a page in system memory to form a reserved page;

writing the reserved page;

selecting a region in the system memory for the translation control entry table; and

initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page.

2. The method of claim 1, further comprising:

updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver.

3. The method of claim 2, further comprising:

restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system.

4. The method of claim 2, further comprising:

determining whether a direct memory address translation corresponding to the entry has been cached in a translation lookaside buffer; and

responsive to a determination that such a direct memory address translation exists, clearing the direct memory address translation from the translation lookaside buffer.

5. The method of claim 1, wherein the page in the system memory is inaccessible to an operating system running on the data processing system.

6. The method of claim 1, wherein writing the reserved page includes setting all bytes within the reserved page to 0xFF.

7. The method of claim 1, wherein initializing all entries to be valid includes setting all valid bits to "1".

9. The method of claim 1, wherein the translation control entry table comprises a 2MB Translation Control Entry table having 512K 4-byte entries.

10. A data processing system for providing valid translation entries in a translation control entry table for all supported direct memory addresses, comprising:

reserving means for reserving a page in system memory to form a reserved page;

writing means for writing the reserved page;

selecting means for selecting a region in the system memory for the translation control entry table; and

initializing means for initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page.

11. The data processing system of claim 10, further comprising:

updating means for updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver.

12. The data processing system of claim 11, further comprising:

restoring means for restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system.

13. The data processing system of claim 11, further comprising:

determining means for determining whether a direct memory address translation corresponding to the entry has been cached in a translation lookaside buffer; and

clearing means for clearing the direct memory address translation from the translation lookaside buffer in response to a determination that such a direct memory address translation exists.

14. The data processing system of claim 10, wherein the reserved page is inaccessible to an operating system running on the data processing system.

15. The data processing system of claim 10, wherein writing the reserved page includes setting all bytes within the reserved page to 0xFF.

16. The data processing system of claim 10, wherein initializing all entries to be valid includes setting all valid bits to "1".

18. The data processing system of claim 10, wherein the translation control entry table comprises a 2MB Translation Control Entry table having 512K 4-byte entries.

19. A computer program product in a recordable-type medium for providing valid translation entries in a translation control entry table for all supported direct memory addresses, comprising:

first instructions for reserving a page in system memory to form a reserved page;

second instructions for writing the reserved page;

third instructions for selecting a region in the system memory for the translation control entry table; and

fourth instructions for initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page.

20. The computer program product of claim 19, further comprising:

fifth instructions for updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver.

21. The computer program product of claim 20, further comprising:

sixth instructions for restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system.

22. The computer program product of claim 20, further comprising:

sixth instructions for determining whether a direct memory address translation corresponding to the entry has been cached in a translation lookaside buffer; and

seventh instructions for clearing the direct memory address translation from the translation lookaside buffer in response to a determination that such a direct memory address translation exists.

23. The computer program product of claim 19, wherein the reserved page is inaccessible to an operating system running on the data processing system.

24. The computer program product of claim 19, wherein writing the reserved page includes setting all bytes within the reserved page to 0xFF.

25. The computer program product of claim 19, wherein initializing all entries to be valid includes setting all valid bits to "1".

27. The computer program product of claim 19, wherein the translation control entry table comprises a 2MB Translation Control Entry table having 512K 4-byte entries.

28. The method of claim 1, wherein the reserved page is utilized for direct memory access address translation.

29. The data processing system of claim 10, wherein the reserved page is utilized for direct memory access address translation.

30. The computer program product of claim 19, wherein the reserved page is utilized for direct memory access address translation.

EVIDENCE APPENDIX

There is no evidence to be presented.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.